



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

09/916,598

07/26/2001

Padmanabha I. Venkitakrishnan

10008009

8711

7590 08/01/2008  
HEWLETT-PACKARD COMPANY  
Intellectual Property Administration  
P.O. Box 272400  
Fort Collins, CO 80527-2400

EXAMINER

KNOLL, CLIFFORD H

ART UNIT

PAPER NUMBER

2111

MAIL DATE

DELIVERY MODE

08/01/2008

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

---

BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

---

*Ex parte* PADMANABHA I. VENKITAKRISHNAN,  
SHANKAR VENKATARAMAN, PAUL KELTCHER,  
STUART C. SIU, STEPHEN E. RICHARDSON, and  
GARY LEE VONDRAN, JR.

---

Appeal 2008-0465  
Application 09/916,598  
Technology Center 2100

---

Decided: July 31, 2008

---

Before JOSEPH L. DIXON, LANCE LEONARD BARRY, and  
STEPHEN C. SIU, *Administrative Patent Judges*.

DIXON, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the  
Examiner's final rejection of claims 1-20. We have jurisdiction under  
35 U.S.C. § 6(b).

We AFFIRM.

## BACKGROUND

Appellants' invention relates to a cache coherent split transaction memory bus architecture and protocol for a multi processor chip device. A further understanding of the invention can be derived from a reading of exemplary claim 1, which is reproduced below.

1. A cache coherent multiple processor integrated circuit, comprising:

a plurality of processor units;

a plurality of cache units, one of the cache units provided for each one of the processor units;

an embedded RAM unit for storing instructions and data for the processor units;

a cache coherent bus coupled to the processor units and the embedded RAM unit, the bus configured to provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit.

## PRIOR ART

The prior art references of record relied upon by the Examiner in rejecting the appealed claims are:

Sherburne	US 2002/0184546 A1	Dec. 5, 2002 (filed Apr. 18, 2001)
Bitar	US 6,418,460 B1	Jul. 9, 2002 (filed Feb. 18, 1997)

Miller	US 6,560,682 B1	May 6, 2003 (filed Oct. 3, 1997)
Arimilli '322	US 6,571,322 B2	May 27, 2003 (filed Dec. 28, 2000)
Arimilli '926	US 6,587,926 B2	Jul. 1, 2003 (filed Jul. 12, 2001)

### REJECTIONS

Claims 1-4, 7, and 9 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Arimilli '926. Claim 5 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli '926 in view of Arimilli'322. Claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli '926 in view of standard practice of memory implementation, as further evidenced by Miller. Claim 8 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli '926 in view of standard embodiment of a processor, as further evidenced by Bitar. Claims 10-13, 16, and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli '926 in view of the standard practice of integrating circuits, as further evidenced by Sherburne. Claim 14 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli '926 and the standard practice of integration, as applied in claim 10 above, further in view of Arimilli '322. Claim 15 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli '926 and the standard practice of integration, as applied in claim 10 above, further in view of the standard practice of memory implementation, as further evidenced by Miller. Claim 17 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli '926 and the standard practice of integration, as applied in claim 10 above, further in view

of a standard processor embodiment, as evidenced by Miller. Claims 19 and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli '926, in view of standard practice of integration and memory implementation, as evidenced by Sherburne, and further in view of Arimilli '322.

Rather than reiterate the conflicting viewpoints advanced by the Examiner and Appellants regarding the above-noted rejection, we make reference to the Examiner's Answer (mailed Feb. 26, 2007) for the reasoning in support of the rejections, and to Appellants' Brief (filed Mar. 23, 2006) for the arguments thereagainst.

#### OPINION

In reaching our decision in this appeal, we have carefully considered Appellants' Specification and claims, the applied prior art references, and the respective positions articulated by Appellants and the Examiner. As a consequence of our review, we determine the following.

#### 35 U.S.C. § 102

"[A]nticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim . . . ." *In re King*, 801 F.2d 1324, 1326 (Fed. Cir. 1986) (citing *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1457 (Fed. Cir. 1984)). "[A]bsence from the reference of any claimed element negates anticipation." *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565, 1571 (Fed. Cir. 1986).

“A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” *Verdegaal Bros., Inc. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). Analysis of whether a claim is patentable over the prior art under 35 U.S.C. § 102 begins with a determination of the scope of the claim. We determine the scope of the claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction in light of the specification as it would be interpreted by one of ordinary skill in the art. *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004). The properly interpreted claim must then be compared with the prior art.

In rejecting claims under 35 U.S.C. § 102, “[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation.” *Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375-76 (Fed. Cir. 2005) (citation omitted).

With respect to independent claim 1, we find that the Examiner has set forth a sufficient initial showing of anticipation wherein Arimilli ‘926 teaches all of the recited structural elements set forth in independent claim 1. Here, we find the bus of Arimilli ‘926 to be a cache coherent bus since the bus is between the processors, including the cache and cache controller, and the embedded RAM and cache coherency is maintained.

Therefore, we look to Appellants' arguments in the Brief to show error in the Examiner's initial showing of anticipation. Appellants argue that Arimilli ‘926 teaches “snooping is performed by storage devices (or internal processors thereof)” yet Appellants maintain that Arimilli ‘926 does not

teach or suggest that the snooping is for ensuring cache coherency between cache units for processors and an embedded RAM unit as recited in the claim 1. Appellants argue that Arimilli '926 "teaches sharply away from these claimed features of the invention."

We are confused by Appellants' arguments which seemingly admit that the processor would perform the snooping yet Appellants argue that the bus is not a cache coherency bus. (App. Br. 11). Furthermore, Appellants argue that the teachings of Arimilli '926 teach way from the claimed invention, but the rejection is based upon anticipation and not obviousness. Therefore, an argument to "teaching away" is not persuasive or relevant.

Appellants reiterate the language of the claim concerning the cache coherent bus but do not explain why the bus of Arimilli is not a cache coherent bus. Nor do Appellants identify any significance to the cache coherent snooping commands from the processor units which may distinguish the claimed structural elements of independent claim 1 from that disclosed by Arimilli '926.

Finally, Appellants argue that "an incredible degree of hindsight has been employed in combining the numerous cited references for the purpose of rejecting Appellants' [sic] Claims as proper motivation to combine the cited references is lacking." (App. Br. 12). Again, Appellants argue issues concerning obviousness concerning the teachings of Arimilli '926 and the claimed invention, but the rejection is based upon anticipation and not obviousness. Therefore, Appellants' arguments are not persuasive of the error in the Examiner's initial showing of anticipation of claim 1. Since Appellants have not provided separate arguments for the patentability of

dependent claims 2-4, 7, and 9, we will sustain the rejection of these dependent claims with representative independent claim 1.

35 U.S.C. § 103(a)

Section 103 forbids issuance of a patent when “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.”

*KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1734 (2007).

In *KSR*, the Supreme Court emphasized "the need for caution in granting a patent based on the combination of elements found in the prior art," *Id.* at 1739, and discussed circumstances in which a patent might be determined to be obvious. *KSR*, 127 S. Ct. at 1739 (citing *Graham v. John Deere Co.*, 383 U.S. 1, 12 (1966)). The Court reaffirmed principles based on its precedent that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Id.* The operative question in this "functional approach" is thus "whether the improvement is more than the predictable use of prior art elements according to their established functions." *Id.* at 1740.

The Federal Circuit recently recognized that "[a]n obviousness determination is not the result of a rigid formula disassociated from the consideration of the facts of a case. Indeed, the common sense of those skilled in the art demonstrates why some combinations would have been obvious where others would not." *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1161 (Fed. Cir. 2007) (citing *KSR*, 127 S. Ct. 1727,



1739 (2007)). The Federal Circuit relied in part on the fact that Leapfrog had presented no evidence that the inclusion of a reader in the combined device was “uniquely challenging or difficult for one of ordinary skill in the art” or “represented an unobvious step over the prior art.” *Id.* at 1162 (citing *KSR*, 127 S. Ct. at 1740-41).

One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. *In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986).

With respect to dependent claim 5, Appellants merely reiterate the language of dependent claim 5 and assert that the teachings of Arimilli ‘322 do not remedy the deficiency of Arimilli ‘926. Since Appellants did not show any error or deficiency in the Examiner's rejection with respect to independent claim 1, we do not find Appellants' same argument persuasive of error with respect to dependent claim 5.

With respect to dependent claims 6 and 8, Appellants similarly rely upon the asserted deficiency with respect to independent claim 1. Since Appellants did not show any error or deficiency in the Examiner's rejection with respect to independent claim 1, we do not find Appellants' same argument persuasive of error with respect to dependent claims 6 and 8.

With respect to independent claim 10 and dependent claims 12-18, Appellants reiterate the language of independent claim 10 and generally assert that the secondary references do not remedy the deficiencies of Arimilli ‘926 “outlined above.” Since Appellants did not show any error or deficiency in the Examiner's rejection with respect to independent claim 1

above, we do not find Appellants' same argument persuasive of error with respect to independent claims 10 and its dependent claims 12-18.

With respect to independent claim 19 and dependent claim 20, Appellants reiterate the language of independent claim 19 and generally assert that the secondary references do not remedy the deficiencies of Arimilli '926 "outlined above." Since Appellants did not show any error or deficiency in the Examiner's rejection with respect to independent claim 19 above, we do not find Appellants' same argument persuasive of error with respect to independent claim 19 and its dependent claim 20.

#### CONCLUSION

To summarize, we have sustained the rejection of claims 1-4, 7, and 9 under 35 U.S.C. § 102; and we have sustained the rejection of claims 5, 6, 8, and 10-20 under 35 U.S.C. § 103(a).

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

rwk

HEWLETT-PACKARD COMPANY  
Intellectual Property Administration  
P.O. Box 272400  
Fort Collins, CO 80527-2400